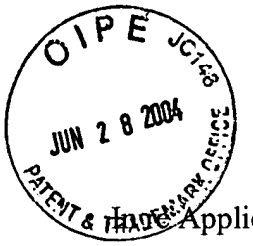
List of designations

100 schematic block diagram of a setup of a semiconductor production installation
101 block of an overall manufacturing process
102 block of a first production area
103 block of a second production area
104 block of a third production area
105 block of a fourth production area
200 semiconductor chip production installation
201 multiplicity of semiconductor chip production sub-installations
202 path of a wafer or a lot through the semiconductor chip production installation
201 machine
301 sensor
302 SECS interface
303 PDSF file
304 log file
306 local communication network (LAN)
307 memory
408 processing step
409 inquiry of the selection criterion
410 test measurement
411 evaluation unit
412 next processing step

"Express Mail" mailing label number EV 314 901 966 US

Date of Deposit: June 28, 2004



Infineon Ref. No. P26994
Our Case No. 10808/113

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

J. Maeritz

Serial No. 10/706,615

Filing Date: November 12, 2003

For METHOD, PREPARATIONS, COMPUTER-READABLE STORAGE AND COMPUTER PROGRAM ELEMENT CONTROL OF PREPARATIONS PROCESS

Examiner: Unknown

Group Art Unit No. Unknown

LETTER TO OFFICIAL DRAFTSMAN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Official Draftsman

Dear Sir:

Please substitute the enclosed 3 sheets of drawings for the previously submitted drawings. The new drawings include English text in place of German text or where text was absent.

Respectfully submitted,

John J. King, Reg. No. 35,918
Attorney for Applicant

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